

A square graphic on the left side of the slide, divided diagonally from the top-left to the bottom-right. The upper-right triangle is green, and the lower-left triangle is black.

CONFIDENTIAL

Future of Supercomputing: The Computational Element

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- **HPC – The New World Order**
- **Whole > Sum-of-Parts?**
- **Key Challenges**
- **A Look Ahead**

All Worldwide Servers Compared To HPC Revenue, Units & Processors

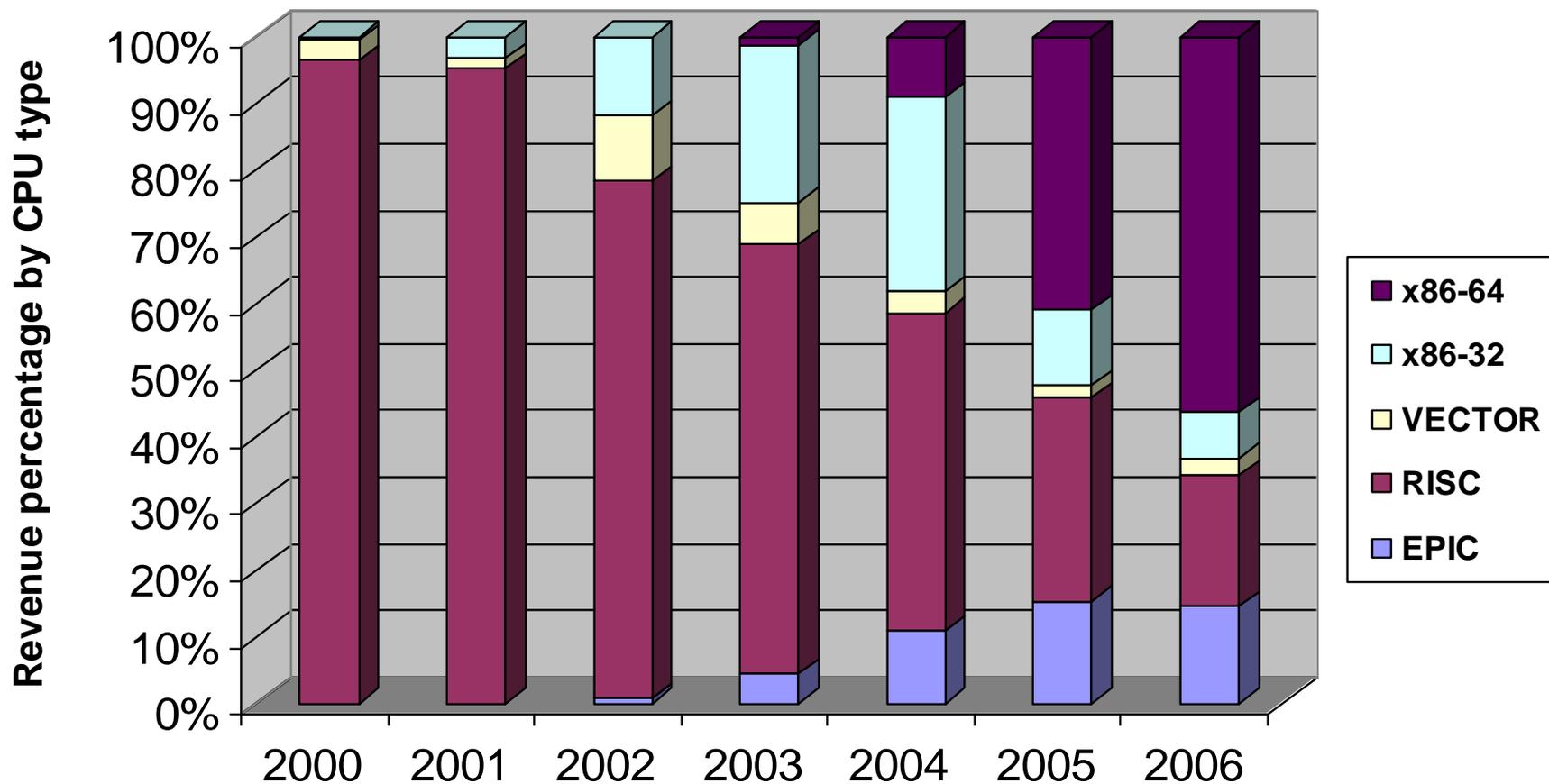


All Servers Worldwide						
	2003	2004	2005	2006	2003 to 2006 CAGR	2005 to 2006 CAGR
Total Factory Revenue (\$B)	\$46,149	\$49,146	\$51,268	\$52,251	4.2%	1.9%
Units Shipped (same as nodes)	5,278,222	6,307,484	7,050,099	7,472,649	12.3%	6.0%
Processor Dies Shipped	8,662,823	10,134,624	11,712,766	12,779,159	13.8%	9.1%
Source: IDC 2007						
HPC Technical Servers Worldwide						
	2003	2004	2005	2006	2003 to 2006 CAGR	2005 to 2006 CAGR
HPC Server Revenue (\$B)	\$5,698	\$7,393	\$9,208	\$10,030	20.7%	8.9%
Adjusted Revenues (To match ente	\$5,128	\$6,654	\$8,287	\$9,027	20.7%	8.9%
Node Units Shipped	411,327	734,510	1,215,735	1,419,221	51.1%	16.7%
Processor Elements Shipped	1,002,905	1,657,827	2,681,079	3,351,843	49.5%	25.0%
Source: IDC 2007						
HPC As A Ratio Of All Servers						
	2003	2004	2005	2006		
Revenue (\$B)	12.3%	15.0%	18.0%	19.2%		
Adjusted Revenues (Apples-to-appl	11.1%	13.5%	16.2%	17.3%		
Units Shipped (Nodes)	7.8%	11.6%	17.2%	19.0%		
Processors Shipped	11.6%	16.4%	22.6%	26.1%		
Source: IDC 2007						



Total HPC Revenue by Processor Type

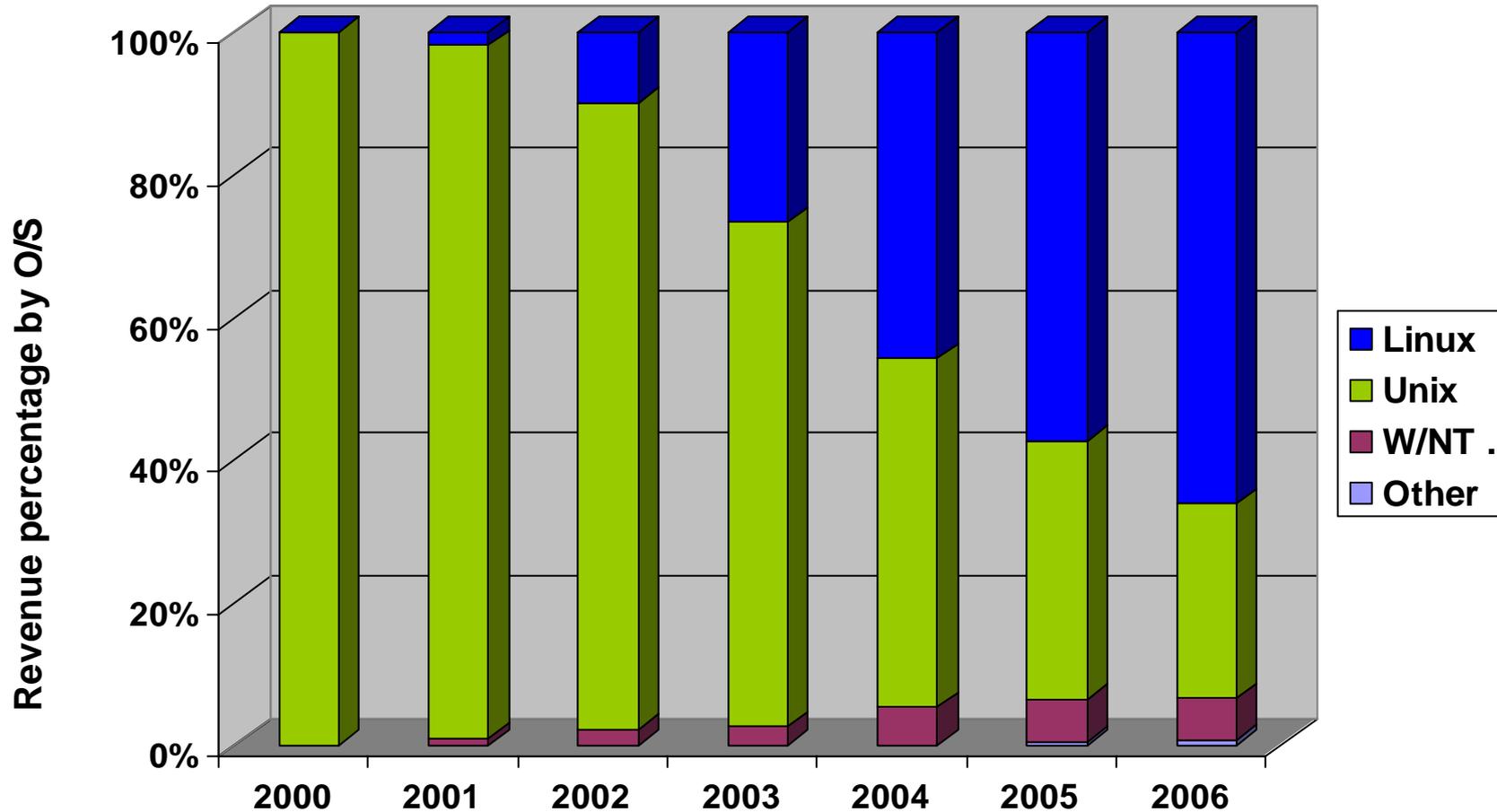
Source: IDC



X86 bases system took 63% share in 2006

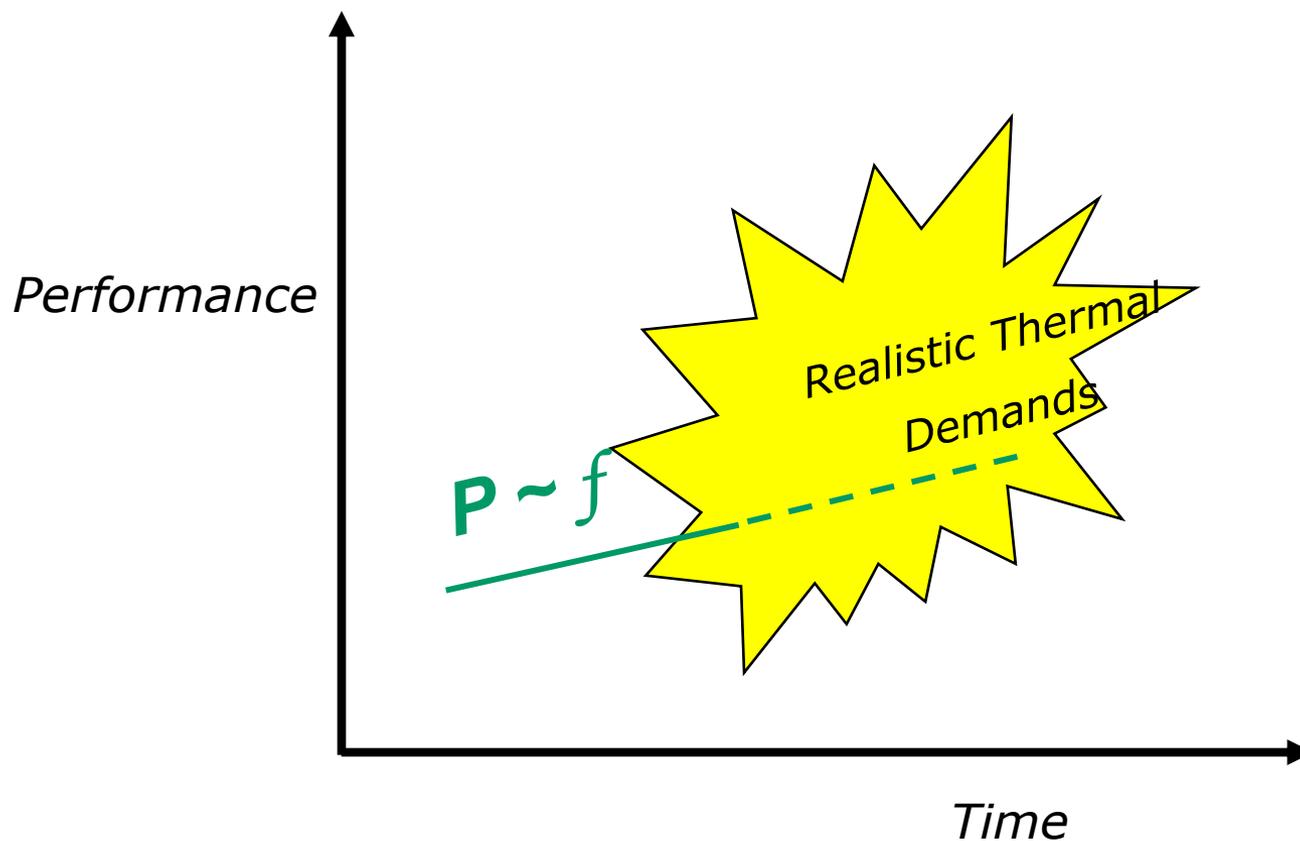
Total HPC Revenue by OS

Source: IDC

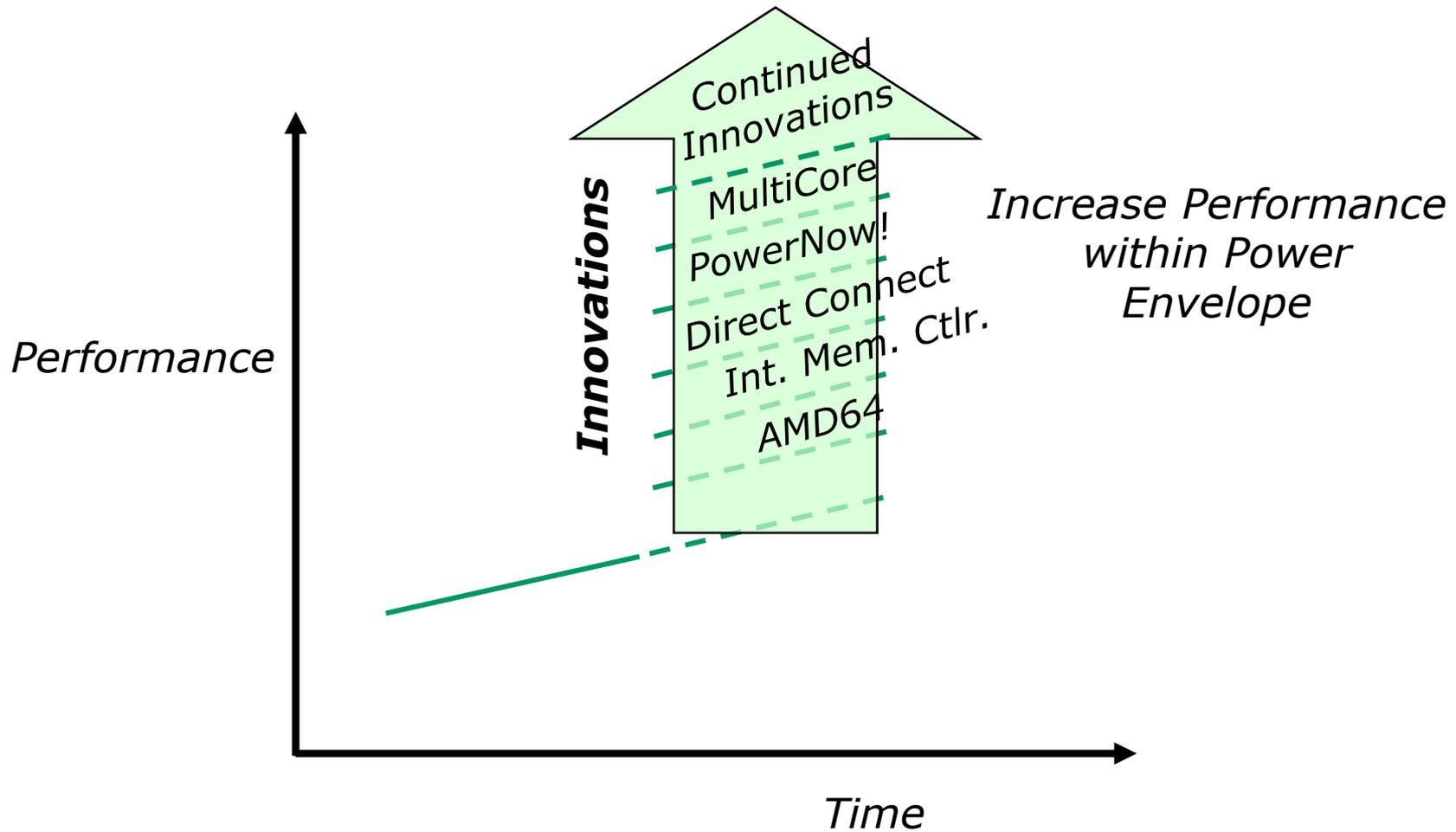


Linux systems accounted for 66% of the total revenue in 2006

Historical Performance Metrics



New Metric: Performance per Watt



Power – The final frontier...

The combined total of data centers in California for 2004 were estimated to require ~300MW of energy.

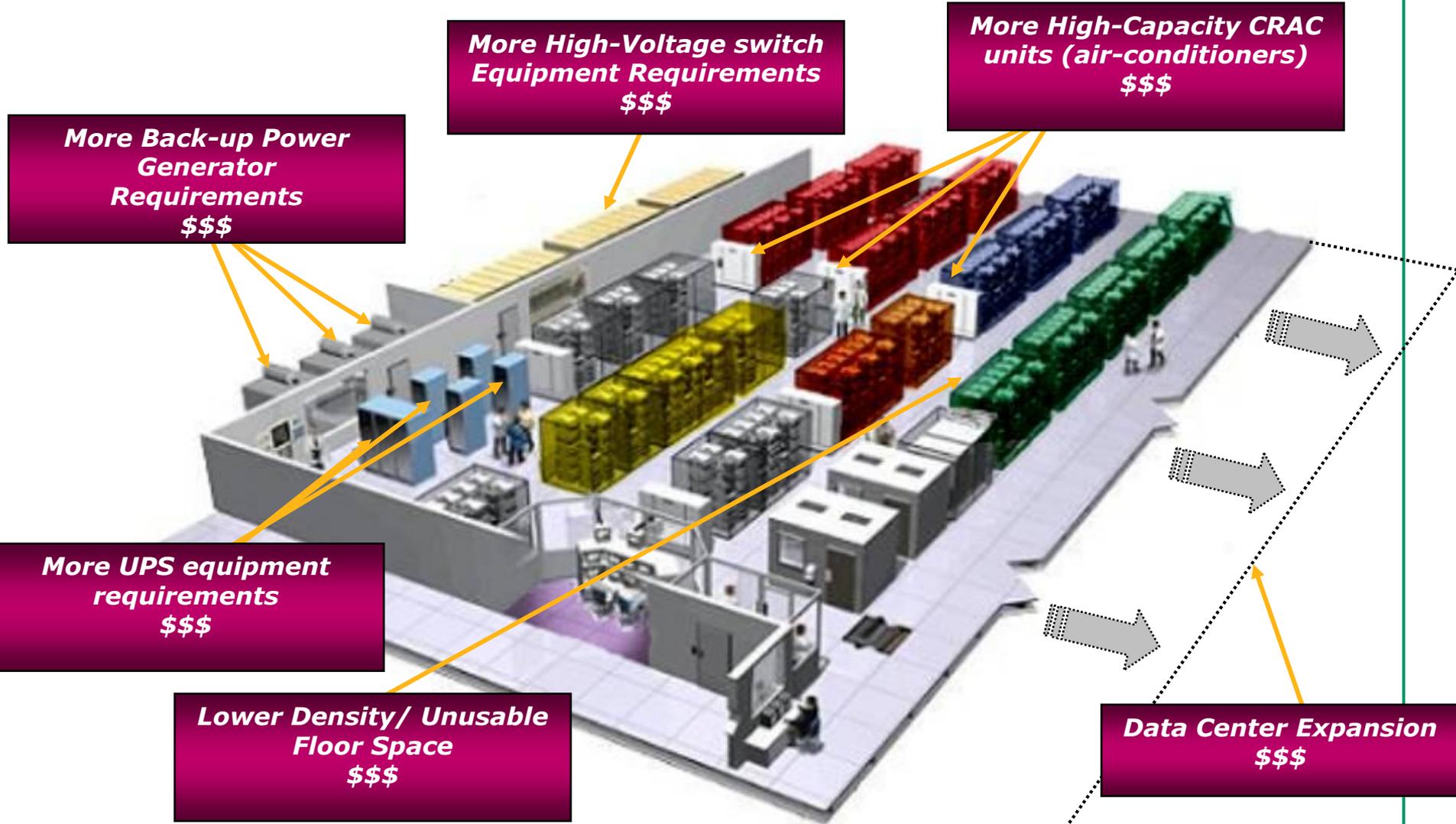
*That's equivalent to
~5000 barrels of oil a day!*



SOURCE: California Energy Commission

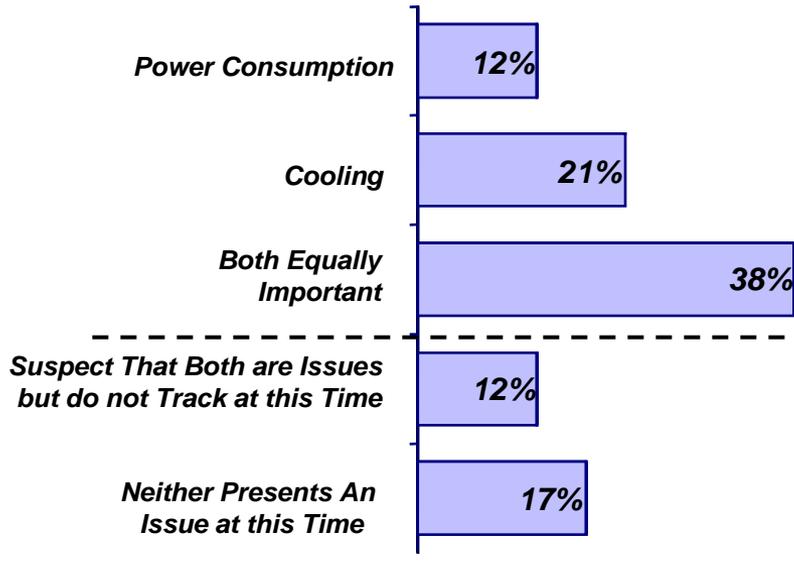
http://www.energy.ca.gov/reports/2004-04-07_500-04-004.PDF

Feeding the Beast (Watts)

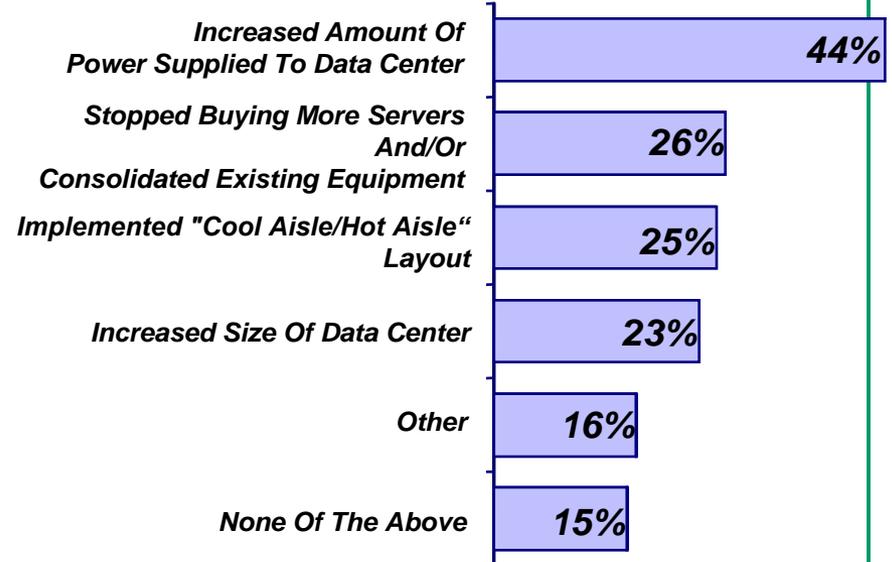


IT Knows it has a Problem

Power Consumption/Cooling Issues Tracked By Company: 71%



How Are Companies Addressing These Issues



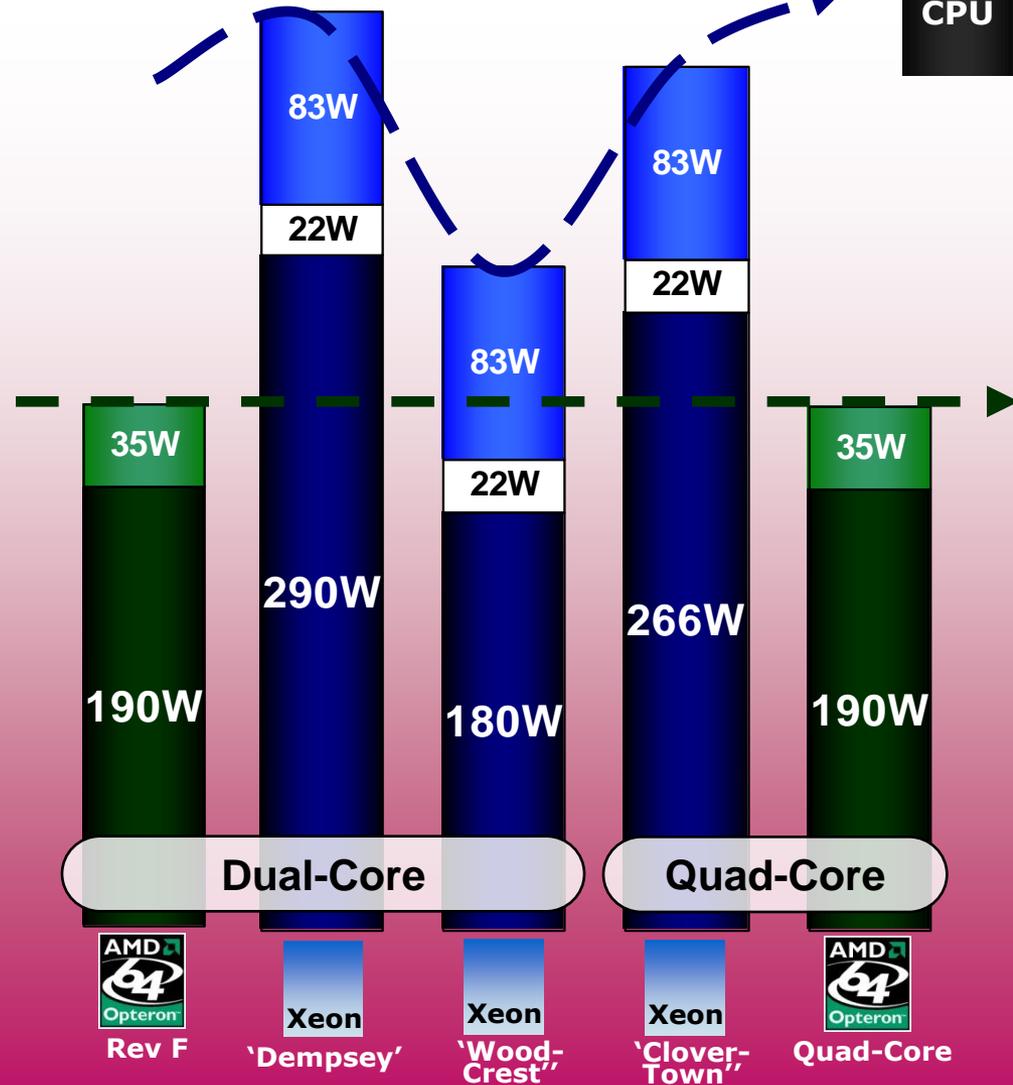
*Base: 1,177 IT Decision Makers November 2005
Strategy Group/Ziff-Davis*

Average of 18% of total rack space wasted due to power and cooling issues

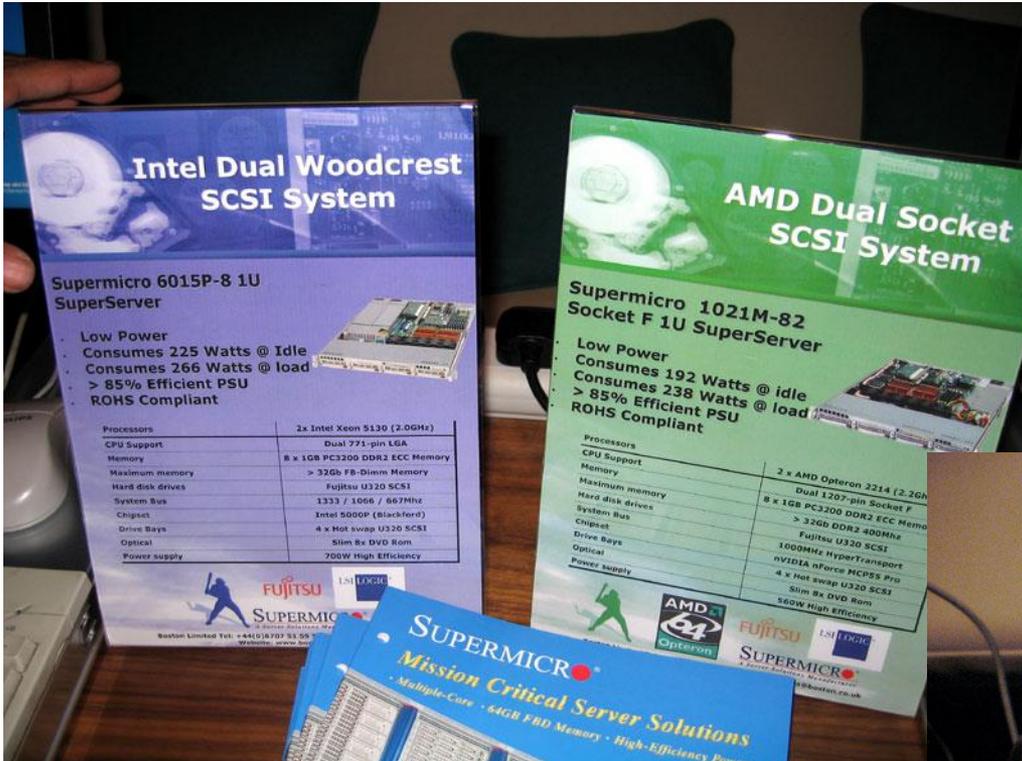
Next-Generation Power Comparison

In 2006 Next-Generation AMD Opteron™ Defined **A New Standard In Performance-Per-Watt** With Energy-Efficient **DDR2 Memory** and **Improved AMD PowerNow!™** Capabilities

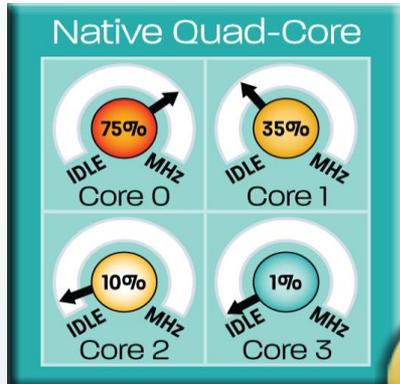
In mid-2007 We Plan to Offer **Quad-Core AMD Opteron** in the Same DDR2-based Platforms at the **Same Power Efficiency**



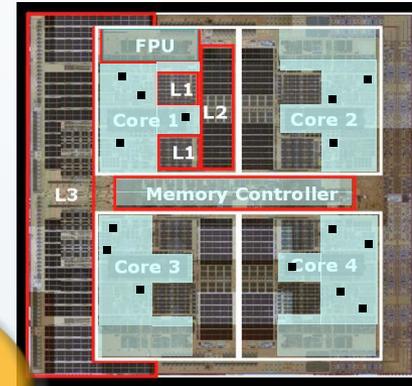
At the Wall Power Comparison



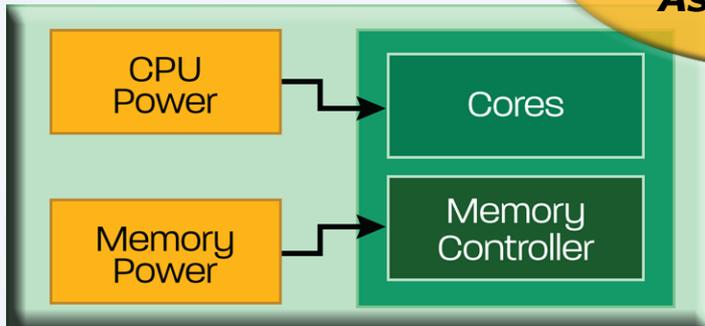
Independent Dynamic Core Technology



AMD CoolCore™ Technology



**Same Power
And Thermal Envelopes
As Dual-Core!**



Dual Dynamic Power Management™



Low-Power DDR2 Memory



What makes a great HPC CPU?

- Great CPU performance, FP and Integer
 - Lots of Cores at good clock rate
 - Maximum throughput per power
- Maximum Cache and Memory bandwidth
 - Each Flop is 2 Reads and 1 Write
 - Ideally 1 Byte/sec per FLOP
- Memory bandwidth must scale with # of cores
 - Otherwise the efficiency of additional cores is low
 - Major challenge beyond 4 cores per socket

A balanced system means to have good
Memory and I/O Bandwidth / FLOP

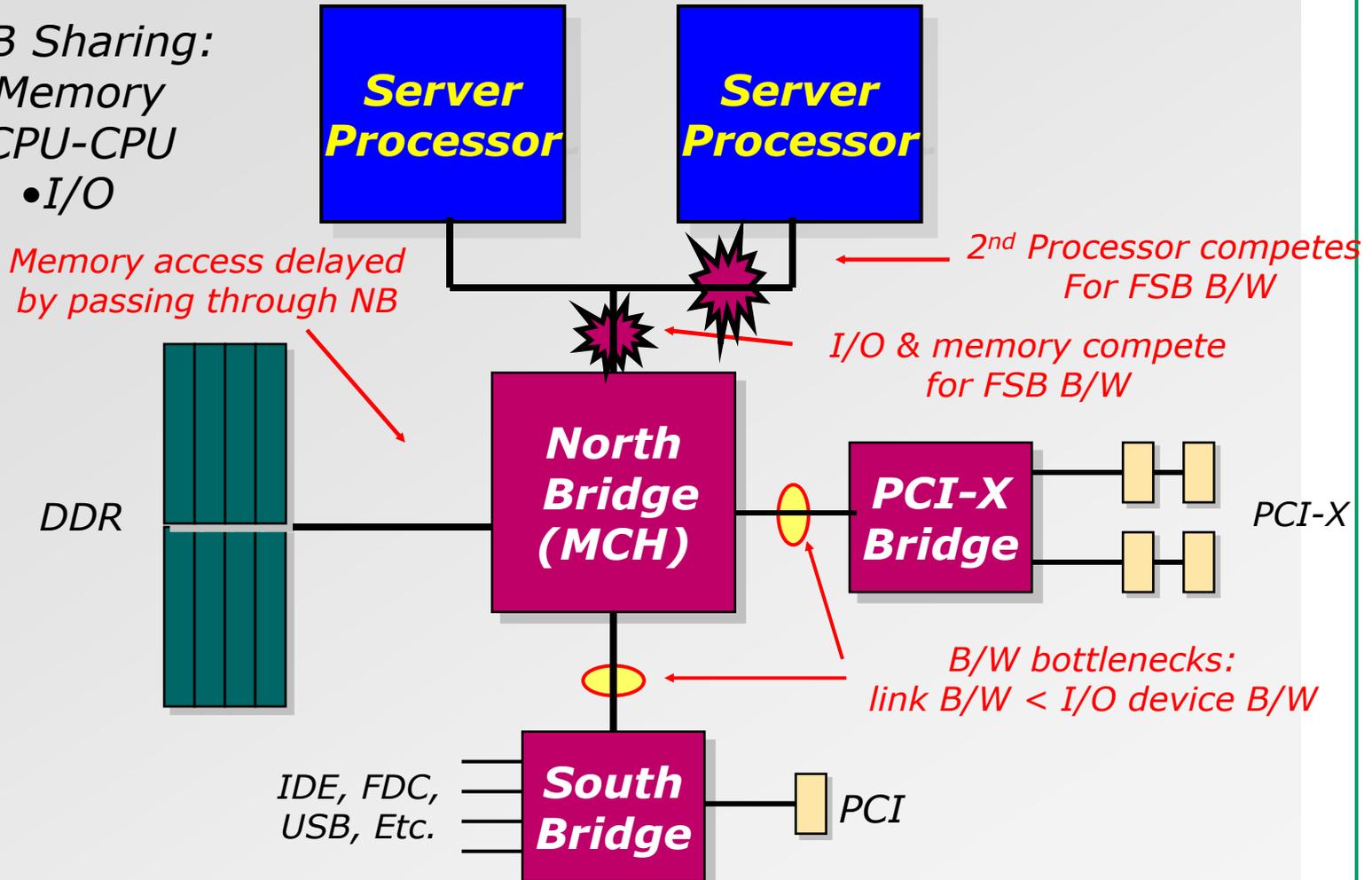
What Makes a Great CPU even better?

-  • Frequency Lift
-  • Instruction Set Enhancement
-  • Increasing Cores
-  • Core Capabilities
-  • Memory Access (Capacity, Bandwidth & Latency)
-  • CPU-CPU connectivity
-  • IO Connectivity (Data access)
-  • Software Scaling

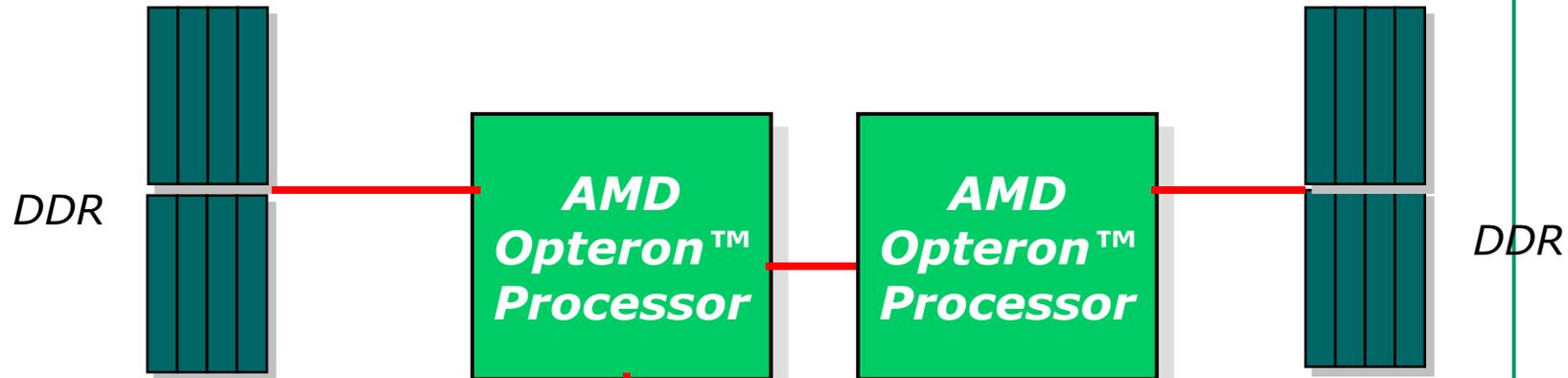
Legacy Northbridge Server Architecture

FSB Sharing:

- Memory
- CPU-CPU
- I/O

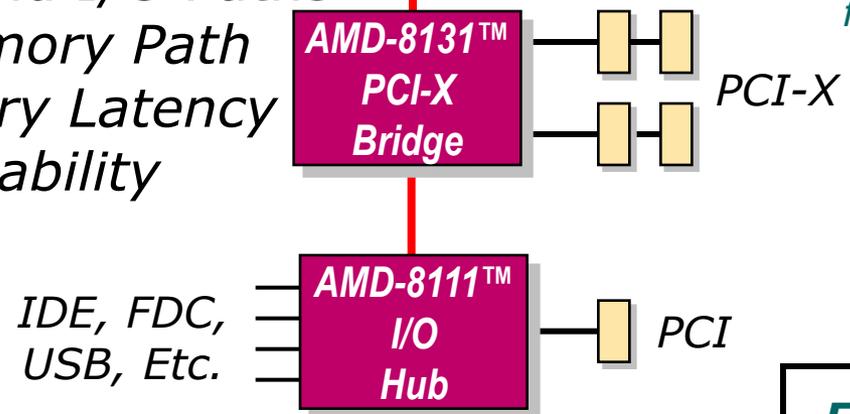


AMD Opteron™ “Direct Connect” Server Architecture



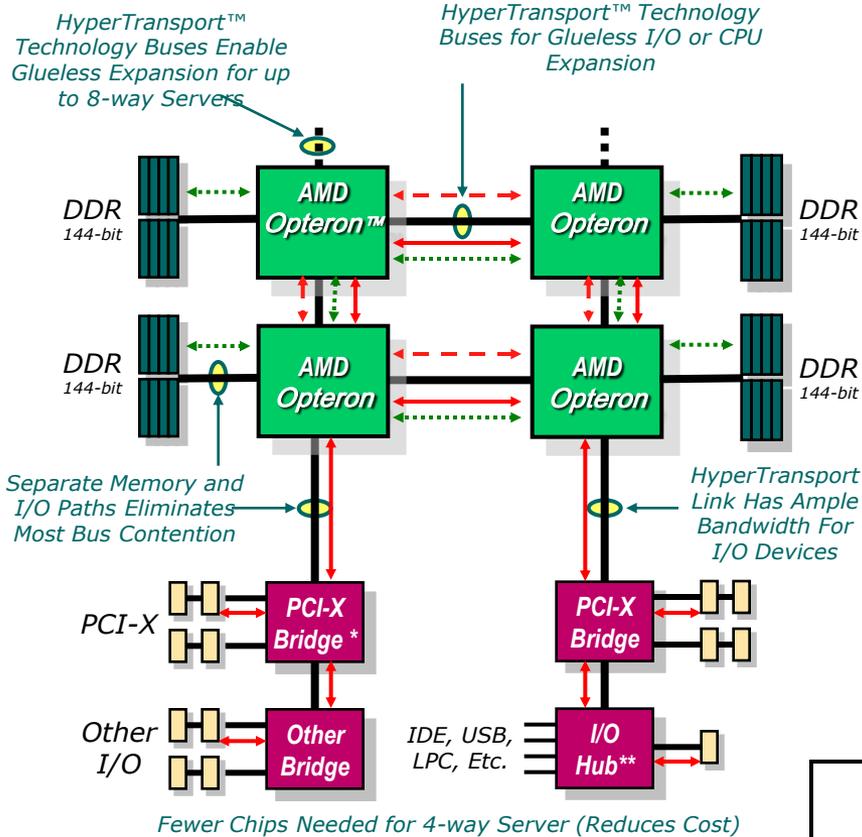
- Reduced Bus Contention
- Separate Mem. And I/O Paths
 - Dedicated Memory Path
 - Reduced Memory Latency
 - Better Scalability

HyperTransport™ bus has ample bandwidth for I/O devices

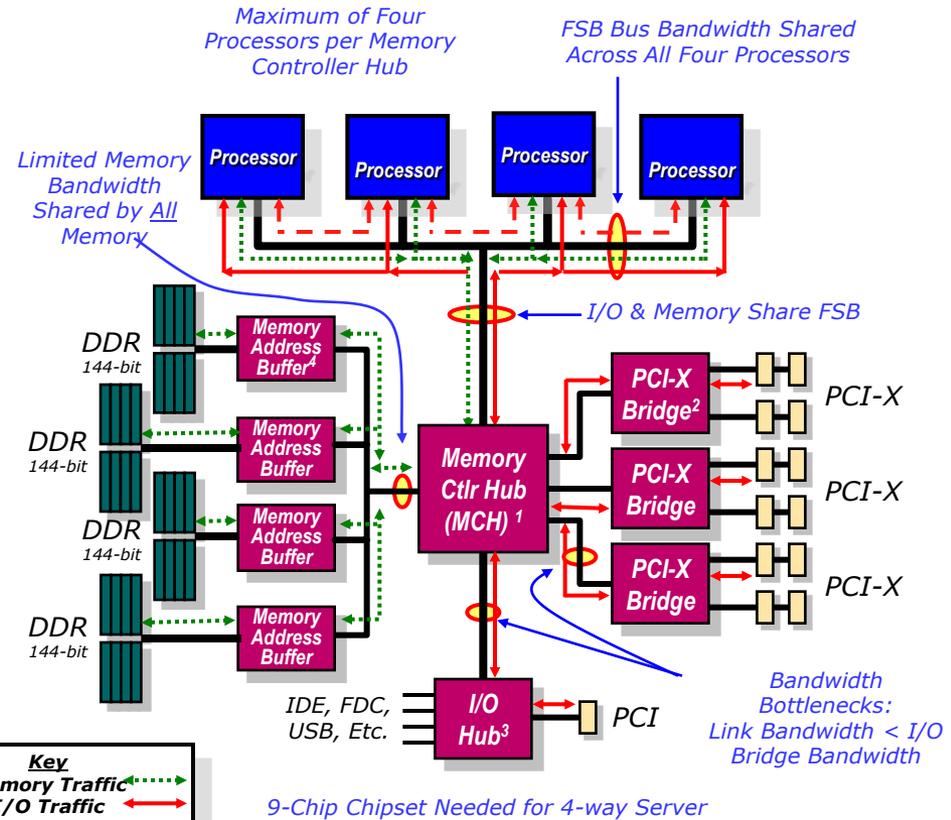


**Fewer chips needed
for basic server**

AMD Opteron™ Platform



Historic MP Server



• Scalable memory and I/O bandwidth

- Up to 8 processors without glue logic
- Each processor adds more memory
- Each processor adds additional HyperTransport™ buses for more PCI-X and other I/O bridges
- Fewer chips required

• System scalability limited by Northbridge

- Maximum of 4 processors
 - o Processors compete for FSB bandwidth
- Memory size and bandwidth are limited
 - Maximum of 3 PCI-X bridges
 - Many more chips required

*AMD-8131™ HyperTransport PCI-X Tunnel **AMD-8111™ HyperTransport I/O Hub

¹ ServerWorks CMIC HE Memory Controller Hub (MCH) ² ServerWorks CIOB-X 64-bit PCI/PCI-X Controller Hub

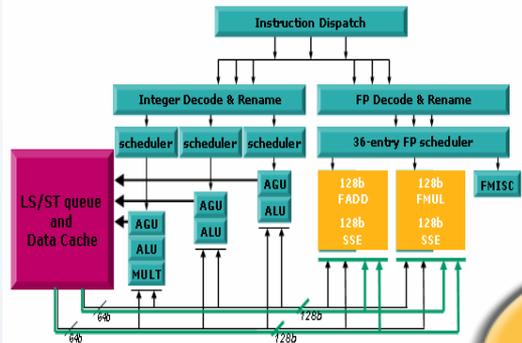
³ ServerWorks CSB5 I/O Controller Hub

⁴ ServerWorks REMC Memory Address Buffer

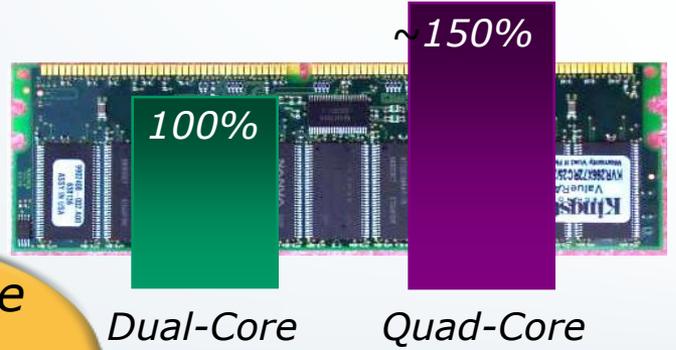


- Dual Dynamic Power Management
- Memory Optimizer Technology
- Wide Floating Point Accelerator

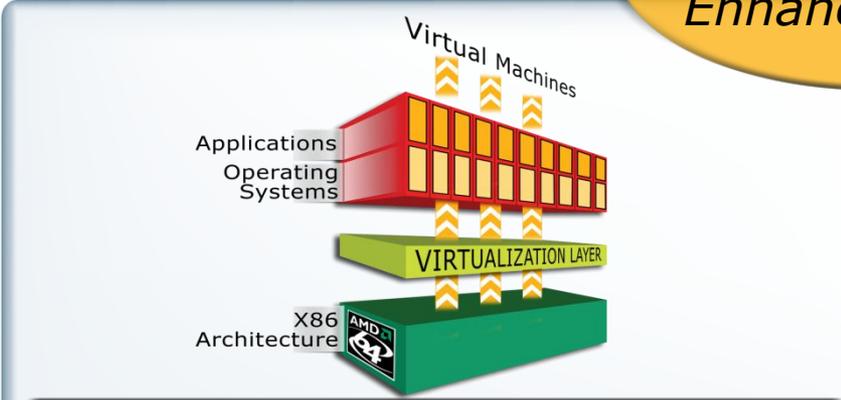
AMD Wide Floating-Point Accelerator



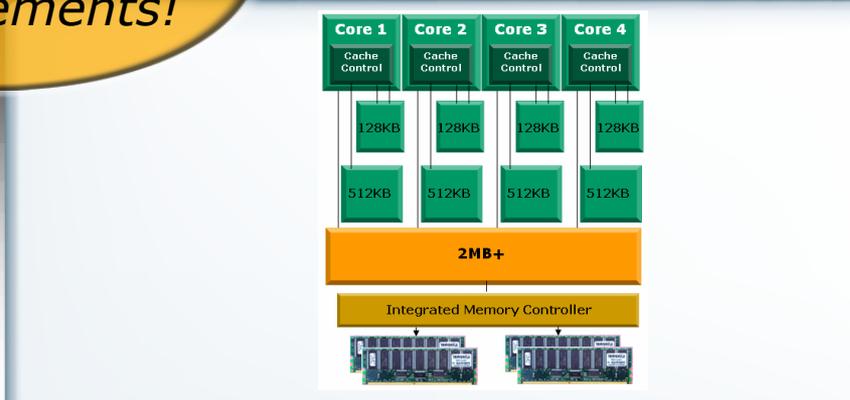
AMD Memory Optimizer Technology



Comprehensive Performance Enhancements!



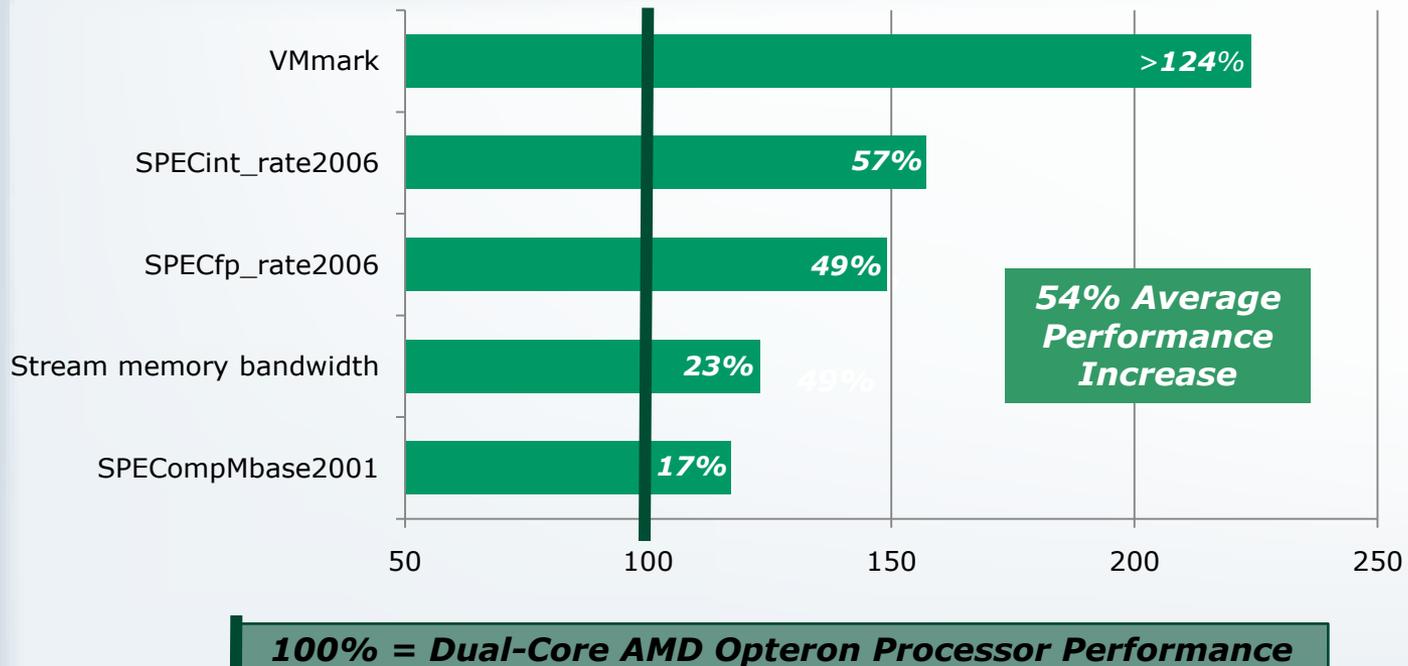
Rapid Virtualization Indexing™



AMD Balanced Smart Cache

Dual-Core to Quad-Core Uplift

Dual-Core AMD Opteron™ 2200 Series vs. Quad-Core AMD Opteron Model 2350 2 Socket Performance Scaling

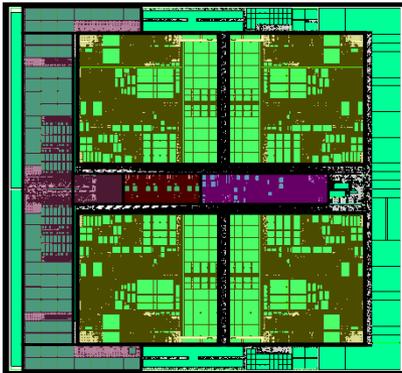


SPEC and the benchmark name SPECint, SPECfp and SPECOMP are registered trademarks of the Standard Performance Evaluation Corporation. Benchmark results stated above for Dual-Core AMD Opteron™ processor Model 2222 reflect results published on www.spec.org as of Sep 9, 2007. The comparison presented above is based on results for Quad-Core AMD Opteron processor Model 2350 under submission to SPEC as of Sep 9, 2007. For the latest results visit <http://www.spec.org/cpu2006/results/> and <http://www.spec.org/omp/results/>. Stream and VMmark results based on internal measurements at AMD performance labs.

Quad-Core vs. Dual-Die

AMD's design will be a TRUE quad-core processor without compromising performance, power or heat

Intel may rush a "dual die" architecture to market in order to claim "first to market", only to change the design to true quad-core later - more churn and increased customer TCO



Native Quad-Core Design

- Optimum performance
- Same power & thermal envelopes as dual-core

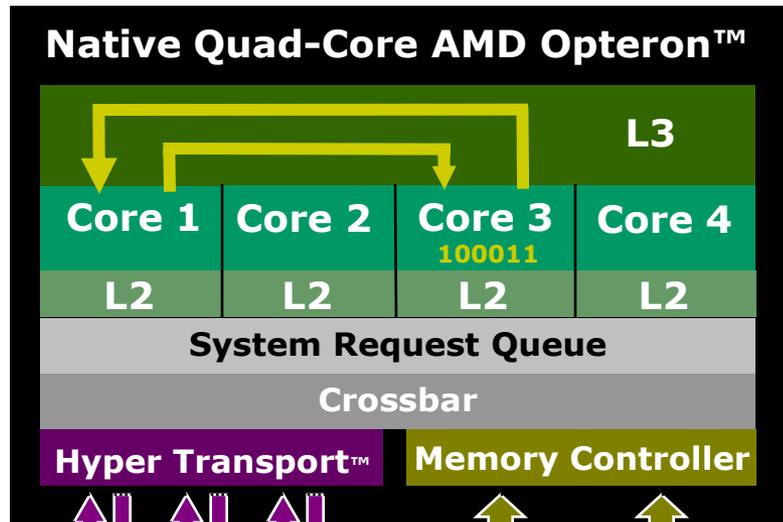


Dual Die (Dual Cavity)

- Can hinder performance (FSB design)
- Publicly known thermal design power ranges higher than dual-core products

Native Quad-Core Benefit: Faster Data Sharing

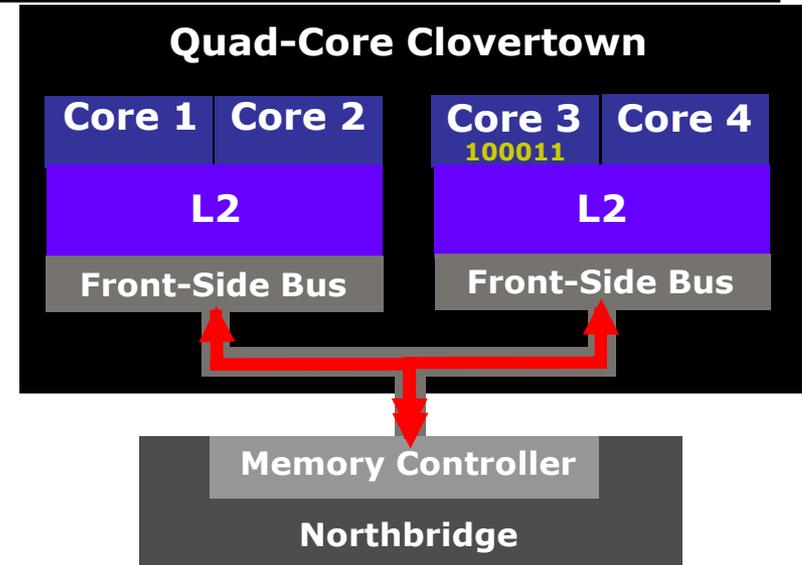
Situation: Core 1 needs data in Core 3 cache ... How Does it Get There?



1. Core 1 probes Core 3 cache, data is copied directly back to Core 1

This happens at processor frequency

**Result: Improved
Quad-Core Performance**



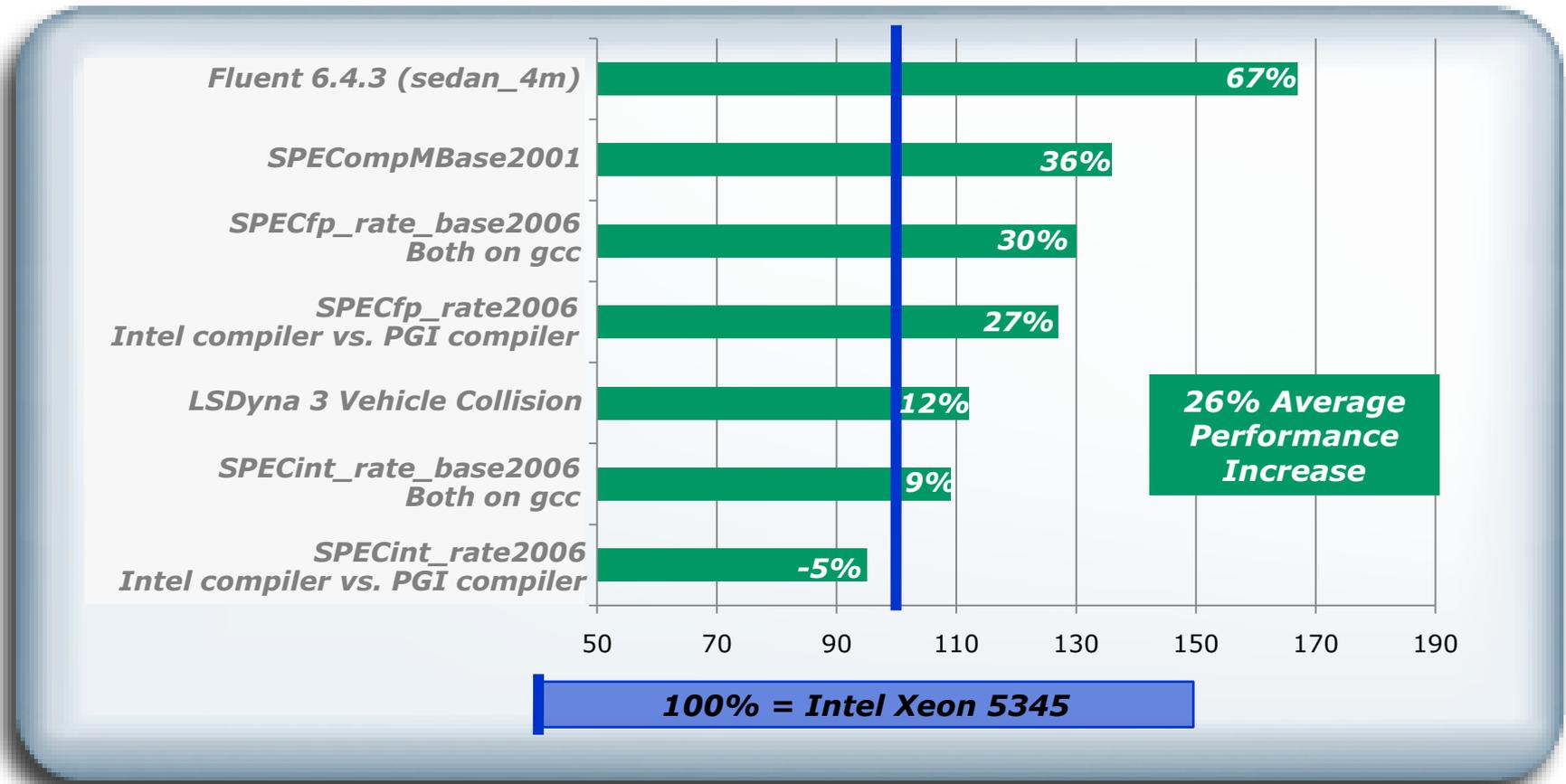
1. Core 1 sends a request to the memory controller, which probes Core 3 cache
2. Core 3 sends data back to the memory controller, which forwards it to Core 1

This happens at front-side bus frequency

**Result: Reduced
Quad-Core Performance**

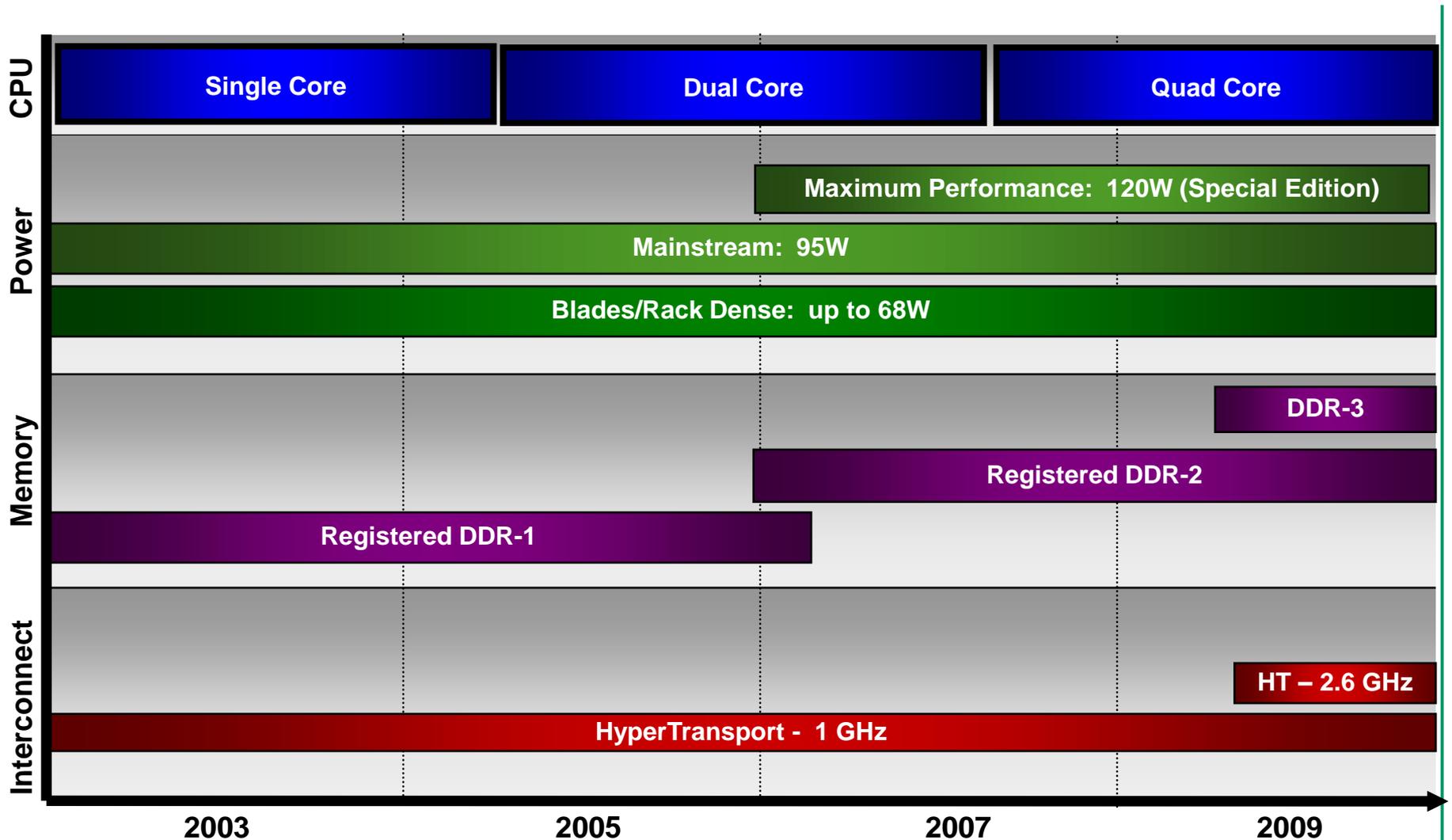
Performance-Per-Watt Leadership

Quad-Core AMD Opteron™ Processor Model 2350 (75 Watt) vs. Intel Xeon 5345 (80 Watt, without Additional Watts of Memory Controller and FBDIMM)



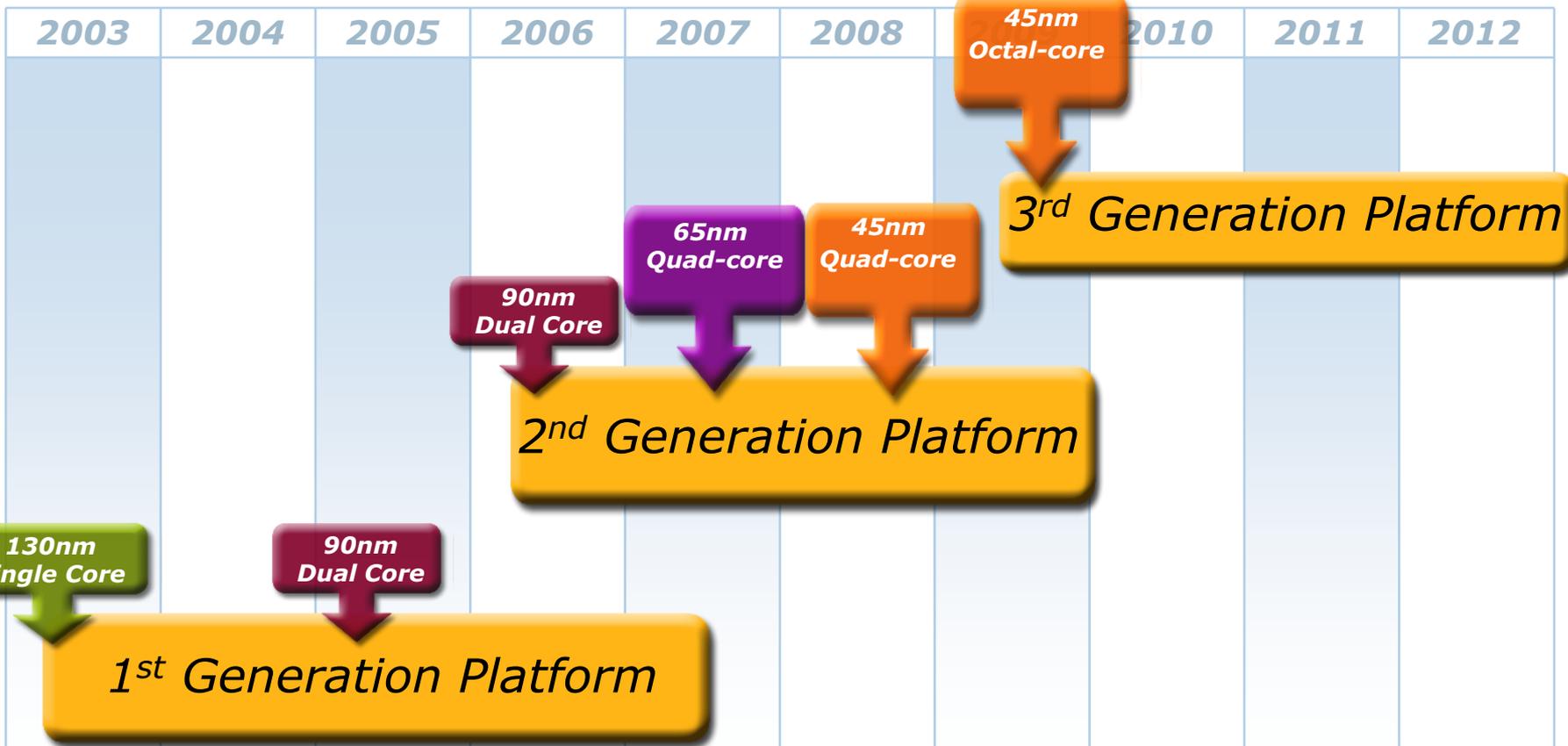
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AMD Server Platform Roadmap



Investment Protection: Stable Platform Progression

Long-term success for partners and end-customers



Platforms in Market Today

2003 vs.

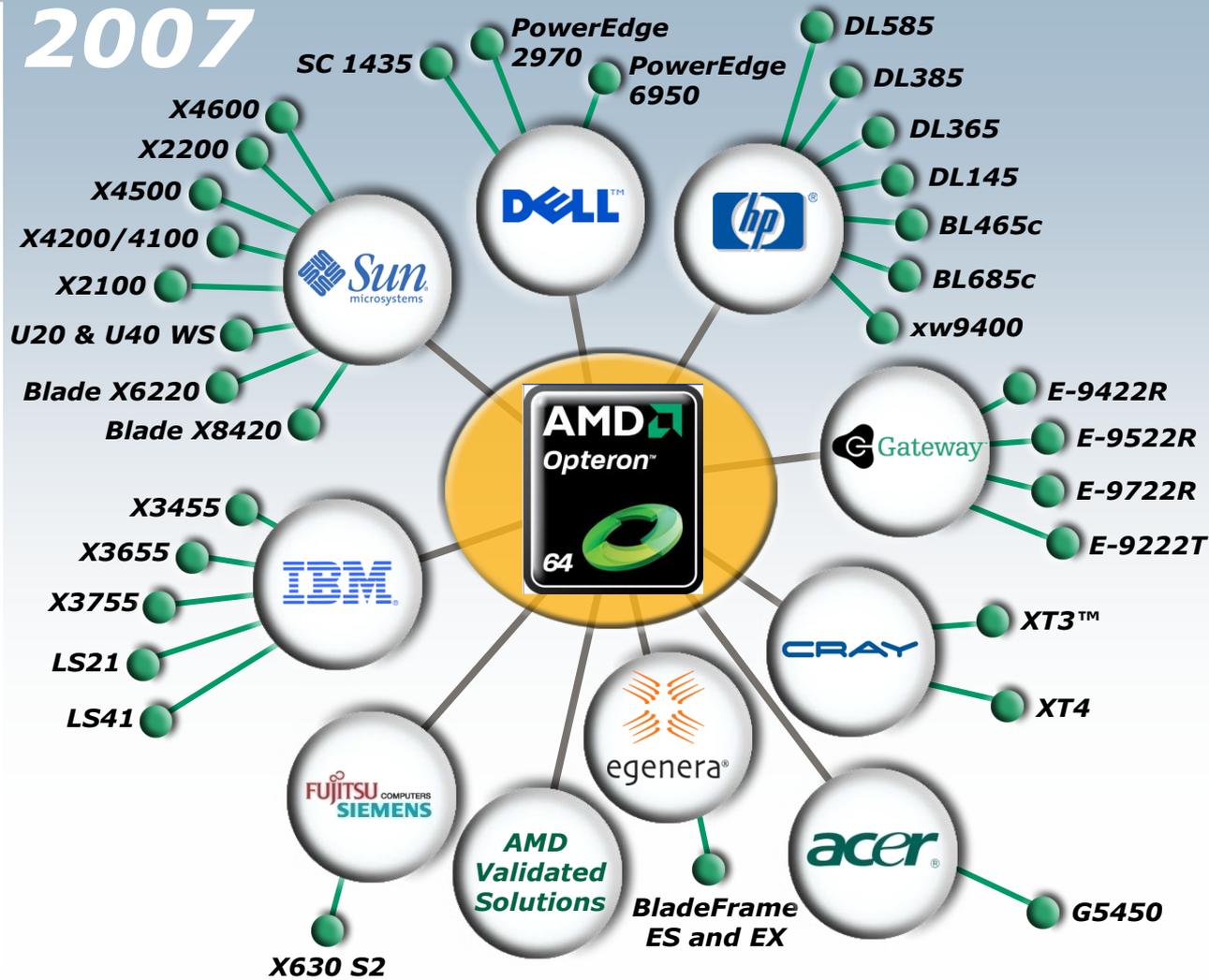


IBM eServer 325



1st Generation AMD Opteron™

2007



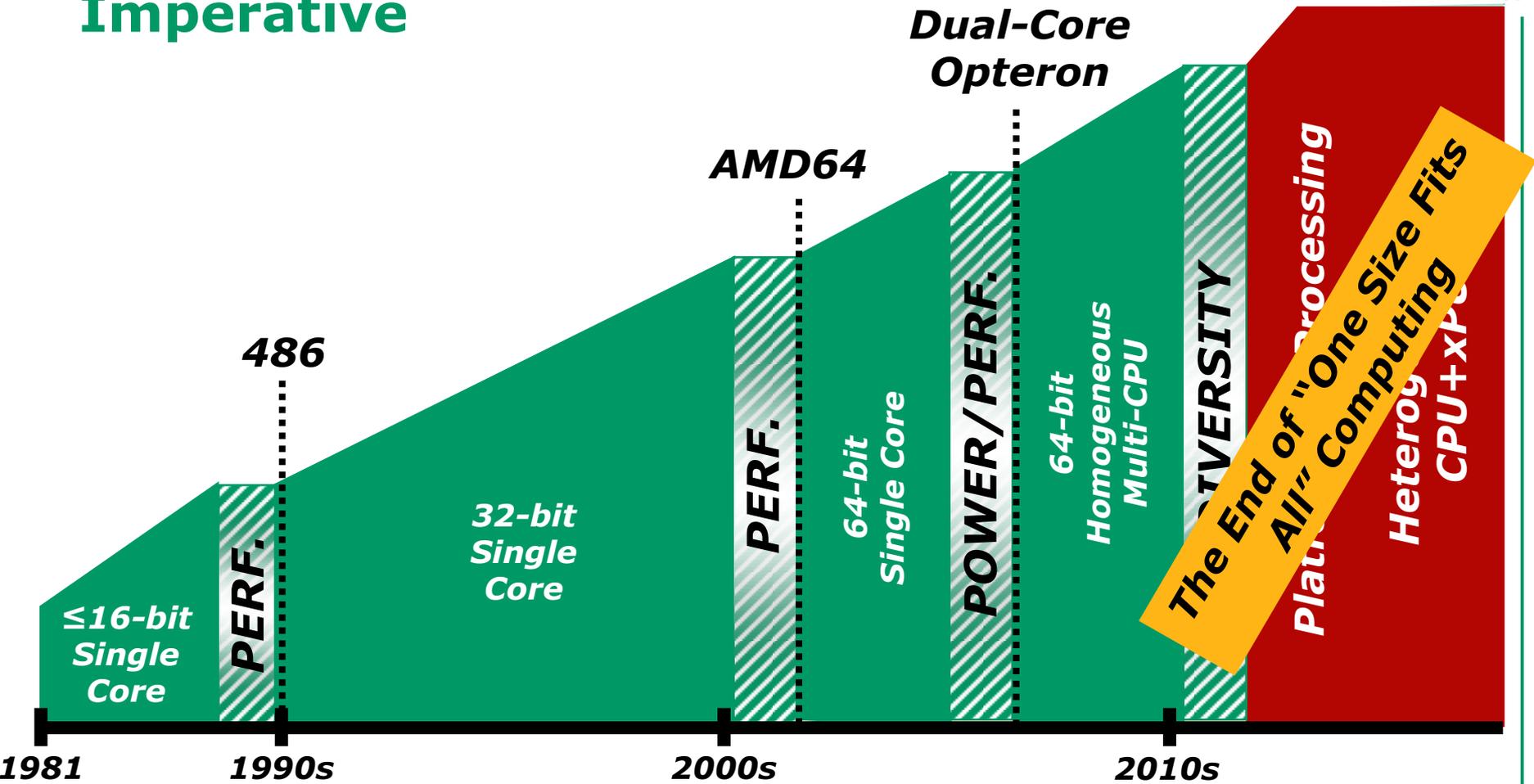
Customers are Responding!

AMD Opteron Server Market Share

	2005	2006
WW total	11.9%	16.0%
WW x86	12.8%	17.1%
WW x86 2-way	13.6%	18.2%
WW x86 4-way	28.2%	40.1%
US x86	20.8%	27.4%
US x86 2-way	21.2%	27.9%
US x86 4-way	36.0%	56.2%

Source: Gartner, IDC, end of year results

The Heterogeneous Processing Imperative



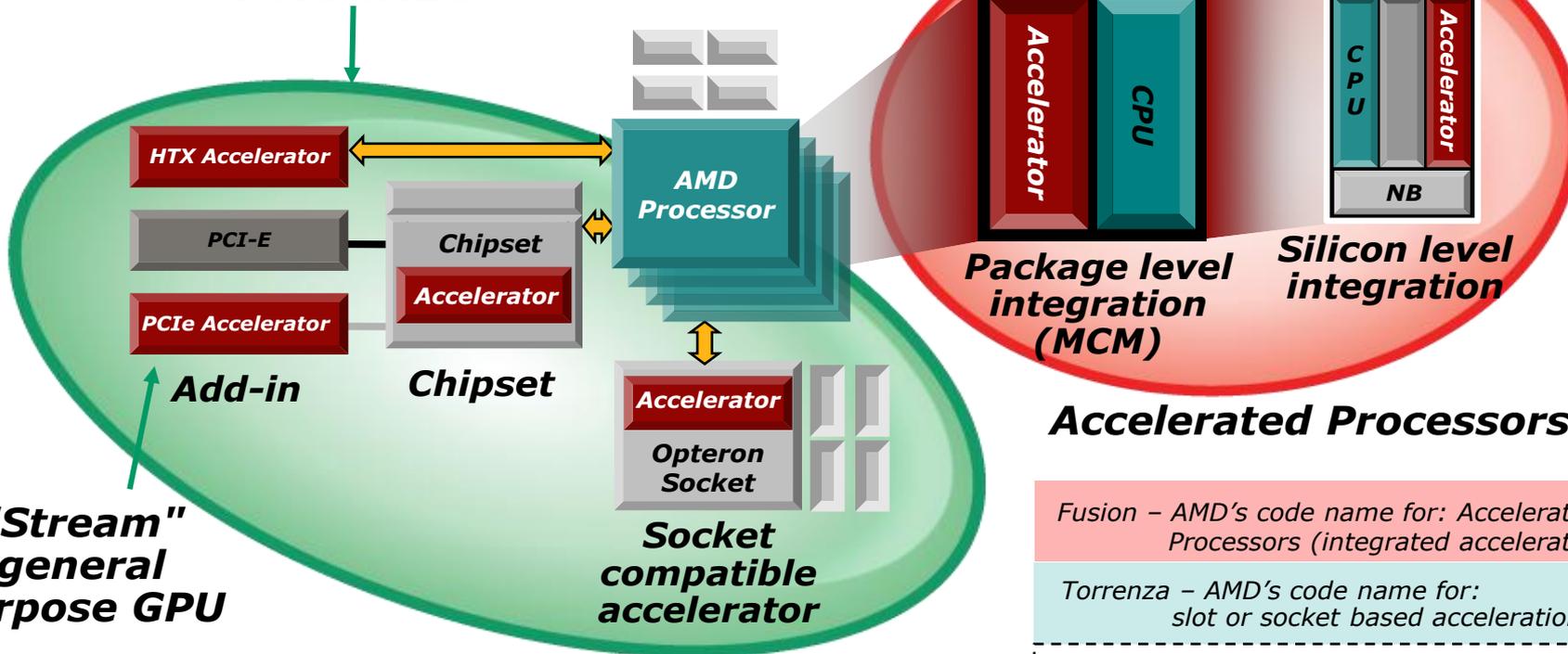
By the end of the decade, homogenous multi-core becomes increasingly inadequate

Continuum of Solutions

Accelerated Computing

"Fusion"

"Torrenza"



Accelerated Processors

Fusion – AMD's code name for: Accelerated Processors (integrated acceleration)

Torrenza – AMD's code name for: slot or socket based acceleration

Stream – Specific example of a GPGPU accelerator under Torrenza

Slot or Socket Acceleration



Torrenza: Accelerated Computing Today

- Direct Connect Accelerators in sockets or slots deliver superior performance without bridge chips
- 100s of GFlops to solve complex math

- Familiar programming interfaces speed time to implementation

Partners:

- Altera
- Celoxica
- DRC
- Lattice
- Xilinx
- XtremeData

- Stream
- ASICs
- FPGA

Compute Offload

- Application Libraries
- Compilers
- Hardware Interfaces

App Programming

Partners:

- CTM
- Celoxica
- OpenFPGA
- Peakstream
- Rapidmind

Torrenza

Partners:

- Bay Microsystems
- Commex
- NetLogic
- Qlogic
- RMI
- Tarari
- Woven

- IB
- XML
- iSCSI
- 10Gb E
- Search
- Storage
- Security

I/O

IT Infra

- Scale Up
- Virtualization

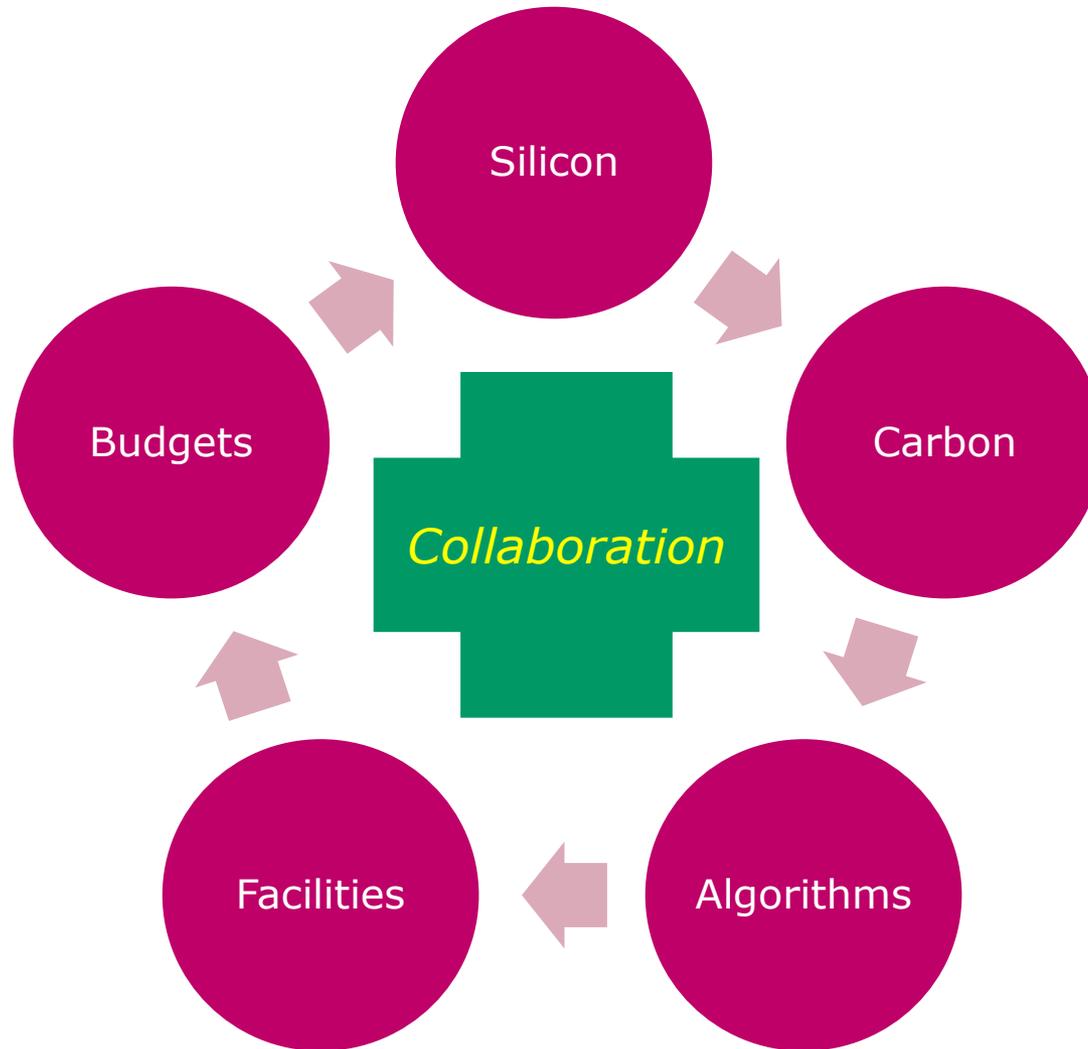
Partners:

- 3Leaf Systems
- Liquid Computing
- Mannheim
- Newisys
- Panta Systems

- Specialized Direct Connect devices for high-throughput, low-latency processing

- cHT and HT provide peer level interfaces to build systems from commodity building blocks

How Do We Get There?



AMD Collaboration Resources

- Green Grid

<http://www.thegreengrid.org/home>

- Developer Pages

<http://developer.amd.com/>

- Torrenza Forum (accelerators)

<http://enterprise.amd.com/us-en/AMD-Business/Technology-Home/Torrenza.aspx>

- Lightweight Profiling for increased parallelism

<http://developer.amd.com/lwp.jsp>

- HyperTransport interconnect

<http://www.hypertransport.org/>

My Prediction...

Texas A&M 38

OSU 13

Gig 'Em Aggies!

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